Notice of Allowability	Application No. 10/604,524	Applicant(s) LEE, HIN-KWAI	
	Examiner Joni Hsu	Art Unit 2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to _papers filed June 10, 2005_.

2. ☒ The allowed claim(s) is/are _1-16 and 18-20_.

3. ☒ The drawings filed on _May 20, 2004 and July 28, 2003_ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Kee M. Tung
Primary Examiner

DETAILED ACTION

Response to Amendment

1. Applicant's arguments, see page 4, filed June 10, 2005, with respect to Claims 1-16 and 18-20 have been fully considered and are persuasive. The rejections under 35 U.S.C. 103(a) of Claims 1-16 and 18-20 have been withdrawn.

2. Applicant argues that paragraphs [0001-0008] of "Background of the Invention section" cited by the Examiner as Applicant's Admitted Prior Art is not prior art. Applicant has described a particular problem in the background section rather than describing prior art. Applicant's Fig. 1 is not labeled "Prior Art" as is customary when describing prior art (page 4).

In reply, the Examiner agrees. Therefore, Claims 1-16 and 18-20 are allowed, as discussed below.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. The application has been amended as follows:

Claim 17 is cancelled.

Allowable Subject Matter

5. Claims 1-16 and 18-20 are allowed.

The following is an examiner's statement of reasons for allowance:

6. The prior art taken singly or in combination do not teach or suggest a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller for larger frame buffers as recited in Claims 1, 10, and 15. Claims 2-9, 11-14, 16, and 18-20 depend from Claims 1, 10, and 15, and therefore also contain allowable subject matter.

7. The closest prior art (Stortz, US005900885A) teaches a DRAM (22, Figure 2) for storing graphics data and a system memory (14) with a buffer extension (42b) for storing graphics data read by the graphics engine when there is not enough room to store it in the DRAM (Col. 2, lines 40-49). However, Stortz does not teach a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller for larger frame buffers.

8. Another prior art (Mattison, US005335322A) teaches a system memory (32, Figure 2) for storing pixels in a frame buffer (Col. 1, lines 28-31) and an optional dedicated frame buffer (40) for storing pixels for larger frame buffer (Col. 3, lines 7-9). However, Mattison does not teach that this optional dedicated frame buffer is an extension of a DRAM.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Schlapp (US005579473A) teaches a graphics system comprising a dynamic-random-access memory (DRAM) for storing graphics data (Col. 4, lines 41-51); a static random-access memory (SRAM) (56, Figure 2) for storing pixels in a frame buffer (Col. 4, lines 59-61); a first bus to the SRAM (pixel operation bus, 112); a second bus to the DRAM (DRAM operation bus, 110); a refresh controller (340, Figure 3; Col. 13, lines 55-63), which is coupled to the SRAM through the arbiter (330) and the first bus (pixel operation bus) (Col. 14, lines 5-9), and coupled to the DRAM through the arbiter and the second bus (DRAM operation bus) (Col. 13, line 64-Col. 14, line 5), for reading pixels from the frame buffer for display to a display device; a graphics engine (70), coupled to the SRAM through the first bus, and coupled to the DRAM through the second bus, for reading and writing graphics data (Col. 3, line 60-Col. 4, line 19); and a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests from the graphics engine to access the DRAM, and also receiving requests from the refresh controller to access the DRAM and requests from the graphics engine to access the SRAM (Col. 13, line 55-Col. 14, line 9), the dual-layer arbiter allowing

simultaneous access of the DRAM and SRAM (Col. 17, lines 20-26) when the refresh controller requests access of the SRAM (Col. 2, lines 8-12; Col. 4, lines 27-35) and the graphics engine requests access of the DRAM (Col. 3, line 60-Col. 4, line 19), but the dual-layer arbiter delaying access of the DRAM by the graphics engine when the refresh controller access the DRAM, whereby the dual-layer arbiter allows simultaneous DRAM and SRAM access or arbitrated access of either the DRAM or the SRAM (Col. 17, lines 39-53), as recited in Claim 1.

Schlapp also teaches a SRAM (56, Figure 2; Col. 3, lines 26-29), and the SRAM inherently stores data as states of a bi-stable circuit, as recited in Claim 2. This is inherent because all SRAM devices store data as states of a bi-stable circuit, according to the definition found on the free-definition website.

Schlapp also teaches that the SRAM has a higher speed than the DRAM (Col. 4, lines 59-61), and therefore has a smaller access time, as recited in Claim 3.

Schlapp also teaches that the first bus (112, Figure 1) is coupled to the refresh controller (340, Figure 3; Col. 2, lines 8-12; Col. 4, lines 27-35; Col. 13, lines 55-63; Col. 14, lines 5-9) and the graphics engine (70, Figure 1; Col. 3, line 60-Col. 4, line 19) and the second bus (110) is coupled to the refresh controller (Col. 4, lines 27-35; Col. 13, line 64-Col. 14, line 5) and the graphics engine (Col. 3, line 60-Col. 4, line 19). Schlapp describes a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests to access the DRAM, and also receiving requests from the graphics engine to access the DRAM and requests to access the SRAM (Col. 13, line 55-Col. 14, line 9), as recited in Claim 4.

Schlapp also teaches that the first bus (112, Figure 1) comprises address and control signals for controlling access to the SRAM (56, Figure 2; Col. 3, lines 26-29); wherein the

second bus (110, Figure 1) comprises address and control signals for controlling access to the DRAM (Col. 3, lines 21-25) (Col. 4, lines 27-35). Schlapp describes a separate bus (98, Figure 2) for providing data to the SRAM and the DRAM (Col. 4, lines 7-19). However, it would be obvious to include data lines in buses 110 and 112 because as can be seen in Figure 2, buses 110 and 112 contain many different signals, so it would be obvious to include the data signal in these buses as well, as recited in Claim 6.

Schlapp also teaches a dual-layer arbitrated graphics system comprising a dynamic-random-access memory (DRAM) for storing graphics data (Col. 3, lines 21-25); a static random-access memory (SRAM) (56, Figure 2) for storing display pixels in a frame buffer (Col. 3, lines 26-29); an SRAM bus (112, Figure 1) for transferring data to and from the SRAM; a DRAM bus (110) for transferring data to and from the DRAM (Col. 4, lines 27-35); a refresh controller (340, Figure 3) coupled to drive display pixels to a display (Col. 2, lines 8-12). Schlapp describes that the first bus (112, Figure 1) is coupled to the refresh controller (340, Figure 3; Col. 2, lines 8-12; Col. 4, lines 27-35; Col. 13, lines 55-63; Col. 14, lines 5-9) and the graphics engine (70, Figure 1; Col. 3, line 60-Col. 4, line 19) and the second bus (110) is coupled to the refresh controller (Col. 4, lines 27-35; Col. 13, line 64-Col. 14, line 5) and the graphics engine (Col. 3, line 60-Col. 4, line 19). Schlapp describes a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests to access the DRAM, and also receiving requests from the graphics engine to access the DRAM and requests to access the SRAM (Col. 13, line 55-Col. 14, line 9). Schlapp describes a dual-layer arbiter (330, Figure 3) is coupled to receive requests from the refresh controller (340; Col. 13, lines 55-63) and requests from the graphics engine (102), for arbitrating access to the SRAM (56, Figure 2; Col. 4, lines 59-61)

when both the refresh controller and the graphics engine request access to the SRAM, and for arbitrating access to the DRAM (Col. 3, line 60-Col. 4, line 19), but allowing simultaneous or parallel access to both the SRAM and to the DRAM when the refresh controller and the graphics engine request access to different memories; wherein the dual-layer arbiter generates the first select signal to the SRAM and the second select signal to the DRAM in response to the dual-layer arbiter arbitrating access or allowing parallel access (Col. 17, lines 20-26), whereby parallel access to the SRAM and to the DRAM is allowed when arbitrating access is not required by requests (Col. 17, lines 39-53), as recited in Claim 10.

Schlapp also teaches a refresh controller request signal, generated by the refresh controller (340, Figure 3; Col. 2, lines 8-12; Col. 13, lines 55-56) and sent to the dual-layer arbiter (330; Col. 13, line 55-Col. 14, line 9), for requesting access to the SRAM (56, Figure 2; Col. 3, lines 26-29) or to the DRAM (Col. 3, lines 21-25) by the refresh controller (Col. 4, lines 27-35). Since the refresh controller accesses both the DRAM and the SRAM, the refresh controller must inherently generate a refresh controller type signal for indicating when access to the SRAM is requested or when access to the DRAM is requested. Schlapp describes a first graphics engine request signal, generated by the first graphics engine (70, Figure 1) and sent to the dual-layer arbiter for requesting access to the SRAM or to the DRAM by the first graphics engine (Col. 3, line 60-Col. 4, line 19). Since the first graphics engine accesses both the DRAM and the SRAM, the first graphics engine must inherently generate a first graphics engine type signal and send it to the dual-layer arbiter, for indicating when access to the SRAM is requested or when access to the DRAM is requested, as recited in Claim 12.

Schlapp also teaches a dual-memory arbitrated graphics sub-system comprising dynamic-random-access memory (DRAM) means for storing graphics data (Col. 3, lines 21-25); static random-access memory (SRAM) means (56, Figure 2) for storing display pixels in a frame buffer (Col. 3, lines 26-29); refresh controller means (340, Figure 3; Col. 13, lines 55-63) for reading the display pixels from the frame buffer and writing the display pixels to a display during a screen refresh (Col. 2, lines 8-12); a graphics engine means (70) for processing the graphics data to generate display pixels or intermediate graphics data (Col. 3, line 60-Col. 4, line 19); first bus means (112, Figure 1) for transferring address and data to the SRAM means; second bus means (110) for transferring address and data to the DRAM means (Col. 4, lines 27-35); arbiter means (330, Figure 3; Col. 13, line 55-Col. 14, line 9) allowing simultaneous access of the SRAM means and the DRAM means (Col. 17, lines 20-26), as recited in Claim 15.

Schlapp also teaches that a first bus means (112, Figure 1) is further for transferring control signals to the SRAM means (56, Figure 2; Col. 3, lines 26-29) (Col. 4, lines 27-35); wherein the second bus means (110, Figure 1) is further for transferring control signals to the DRAM means (Col. 3, lines 21-25; Col. 4, lines 27-35); wherein the first bus means and the second bus means differ in control signals, as recited in Claim 16.

11. Yamashita (US006313844B1) teaches a graphics system comprising a DRAM (16, Figure 9; Col. 14, lines 18-21), a SRAM (17; Col. 15, lines 8-19), a refresh controller (30; Col. 16, lines 41-45), and a graphics engine (12; Col. 15, lines 24-31). Yamashita describes that the DRAM stores data as charges on capacitors that periodically require refreshing of the charges (Col. 1, lines 37-43), as recited in Claim 2.

Yamashita also teaches that the arbiter means (13, Figure 9; Col. 15, line 41-Col. 16, line 9) further comprises priority means for selecting the refresh controller means (30; Col. 16, lines 41-45) as the first winning requestor when other devices also generate a first request during the same time period (Col. 1, lines 58-62), as recited in Claim 20.

12. Rodgers (US006131140A) teaches a first mux (201a, Figure 3a) connecting the SRAM (105a) to other components (Col. 6, line 66-Col. 7, line 4) and a second mux (208) connecting the DRAM (109, Figure 2) to other components (Col. 8, lines 39-46), as recited in Claim 4.

13. Laksono (US006288729B1) teaches a second graphics engine (Col. 5, lines 57-62) coupled to the system memory (16, Figure 1) through the first bus (22), and coupled to the graphics memory (20) through the second bus, for reading and writing graphics data; wherein the dual-layer arbiter (26) further receives requests from the second graphics engine to access the graphics memory, and requests from the second graphics engine to access the system memory (Col. 4, lines 35-38), and the dual-layer arbiter is connected to the second graphics engine, the system memory, and the graphics memory. It is well-known in the art that the system memory is usually SRAM and the graphics memory is usually DRAM, so the system memory is considered to be SRAM and the graphics memory is considered to be DRAM, as recited in Claim 8.

14. Lavelle (US006812929B2) is similar to Schlapp and teaches a DRAM (914, Figure 8) for storing graphics data and a SRAM (930) for storing pixels in a frame buffer (Col. 10, lines 47-

49). Lavelle also describes that the graphics engine is a video overlay engine (190, Figure 6; Col. 9, lines 33-38), as recited in Claim 9.

15. Kotzur (US006389480B1) teaches a dual-layer arbiter (504, Figure 5A; Col. 18, lines 53-55) that arbitrates access using round-robin arbitration (Col. 2, line 58-Col. 3, line 29; Col. 19, lines 3-5; Col. 28, line 64-Col. 29, line 25) wherein the refresh controller (210, Figure 4) and other ports are given equal priority for accessing the SRAM (650, Figure 6) or the DRAM (638), as recited in Claim 11.

Therefore, Kotzur also inherently teaches receiving first requests for access of the SRAM means from the refresh controller means or other ports, and receiving second requests for access of the DRAM means for the refresh controller means or the other ports, for arbitrating among the first requests when received at a same time period to generate a first grant to a first winning requestor, and for arbitrating among the second requests when received at a same time period to generate a second grant to a second winning requestor, first selector means, for selecting the refresh controller means or the other ports for connection to the SRAM means in response to an indication of the first winning requestor from the arbiter means; and second selector means, coupled to the second bus means, for selecting the refresh controller means or the other ports for connection to the DRAM in response to an indication of the second winning requestor from the arbiter means, whereby three requestors are arbitrated for access of two memories, as recited in Claim 15.

Kotzur teaches a refresh controller and other ports, and a round-robin arbitration for selecting the ports, as discussed above. By definition, a round-robin arbitration has a first round-

robin means for alternately selecting as a first winning requestor the refresh controller means or the other ports; and second round-robin means for alternately selecting as the second winning requestor the refresh controller means or the other ports, as recited in Claim 19.

16. Kato (US006070205A) teaches a DRAM refresh controller (1315, Figure 8) and a DRAM (1305) connected to the first bus (1317) (Col. 9, lines 2-5) and a data retention circuit or refresh controller for SRAM and a SRAM (132) connected to the second bus (1319) (Col. 9, lines 28-34), and a graphics engine (1302) that is connected to both the first and second buses (Col. 8, line 64-Col. 9, line 2). Kato describes first and second bus grant signals generated by the dual-layer arbiter (1306, 1307; Col. 7, lines 23-24; Col. 9, lines 21-26). Therefore, a refresh controller grant signal must inherently be generated by the dual-layer arbiter and sent to the refresh controller, to indicate that the refresh controller may access a requested memory; a first graphics engine grant signal, generated by the dual-layer arbiter and sent to the first graphics engine, to indicate that the first graphics engine may access a requested memory, as recited in Claim 13.

Kato also teaches that the first bus means and the second bus means differ in width of address (Col. 10, lines 54-62), as recited in Claim 16.

17. Stortz (US005900885A) teaches a DRAM (22, Figure 2) for storing graphics data and a system memory (14) with a buffer extension (42b) for storing graphics data read by the graphics engine when there is not enough room to store it in the DRAM (Col. 2, lines 40-49).

18. Mattison (US005335322A) teaches a system memory (32, Figure 2) for storing pixels in a frame buffer (Col. 1, lines 28-31) and an optional dedicated frame buffer (40) for storing pixels for larger frame buffer (Col. 3, lines 7-9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH